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Description

[A POLYSILICON THIN FILM TRANSISTOR]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority benefit of Taiwan application serial no. 91123797, filed on October 16, 2002.

BACKGROUND OF INVENTION

[0002] Field of Invention

[0003] The present invention relates to a thin film transistor (TFT). More particularly, the present invention relates to a timing control method of a polysilicon thin film transistor.

[0004] Description of Related Art

[0005] Due to rapid progress in electronic technologies, digitized video or imaging devices have become an indispensable product in our daily life. Among video and imaging products, displays are the principle devices used for providing information. Through a display device, a user is able to obtain information or to control various operations. To facilitate the users, most video or imaging equipment is

now designed with a slim and fairly light body. With breakthroughs in opto-electronic technologies and advances in semiconductor fabrication techniques, flat panel type displays such as a thin film transistor liquid crystal display (TFT-LCD) are out in the market.

[0006] Recently, a technique for forming a thin film transistor liquid crystal display fabricated having polysilicon thin film transistors has been developed. The thin film transistor in this type of display has electron mobility much greater than a conventional amorphous silicon (a-Si) type of thin film transistor. Since a display with a smaller thin film transistor and a larger aperture ratio can be produced, a brighter display with lower power consumption is obtained. Moreover, due to the increase in electron mobility, a portion of the driving circuit and the thin film transistor may be fabricated on a glass substrate together at the same time. Thus, reliability and quality of the liquid crystal display panel is improved and the production cost relative to a conventional amorphous silicon type of thin film transistor liquid crystal display is much lower. Furthermore, because polysilicon is a lightweight material with the capacity to produce high-resolution display without consuming too much power, a polysilicon thin film

transistor display is particularly appropriate for installing on a portable product whose body weight and energy consumption is critical.

[0007] Earlier generations of polysilicon thin film transistor were fabricated using solid phase crystallization (SPC) method at temperature higher than 1000°C. With such a high processing temperature, a quartz substrate must be used. Since quartz substrate costs more than a glass substrate and is also subjected to dimensional limitation (not more than 2 to 3 inches in size), polysilicon thin film transistor was only used in small panel display. Later, with the development of laser and maturation of laser crystallization or excimer laser annealing (ELA) techniques, an amorphous silicon film can be easily re-crystallized into polysilicon through a laser scanning operation at a temperature below 600°C. Hence, a glass substrate suitable for forming conventional amorphous silicon TFT-LCD can also be used to fabricate a polysilicon TFT-LCD having larger panel size. Because a lower fabrication temperature is required, this type of polysilicon is often referred to as a low temperature polysilicon (LTPS).

[0008] Fig. 1 is a schematic cross-sectional view of a conventional polysilicon thin film transistor (TFT). As shown in

Fig. 1, a conventional polysilicon thin film transistor 10 typically includes a poly-island layer 102, an oxide gate insulation film 104, a gate 106 and a first and a second inter-layer dielectric (ILD) 108, 109 over a substrate 100. The poly-island layer 102 includes a channel region 102a under the gate 106, a doped source/drain region 102b on each side of the channel region 102a and a lightly doped drain (LDD) region 102c between the channel region 102a and the doped source/drain region 102b. The gate 106 is positioned over the channel region 102a and the oxide gate insulating film 104 is positioned between the gate 106 and the poly-island layer 102. The first inter-layer dielectric 108 covers the gate 106 and the gate insulating film 104. Furthermore, a source/drain contact metal 110 is embedded between the first inter-layer dielectric 108 and the gate insulating film 104 on each side of the gate 106. The source/drain contact metal 110 is electrically connected to the doped source/drain region 102b. The second inter-layer dielectric 109 is positioned over the thin film transistor device.

[0009] However, due to poor production quality of the oxide gate insulating film, most polysilicon thin film transistors have a stress related reliability problem that often occurs in the

transistor device. Figs. 2A and 2B are graphs showing the relationship between drain current (I_D) and gate voltage (V_G) of two conventional polysilicon thin film transistors each having a different poly-island aspect ratio obtained after repeated operations. The graphs are obtained when a drain voltage (V_D) of about 10V is applied to polysilicon thin film transistors with a poly-island layer having a width/length ratio of 30/6 and 60/6 respectively and an oxide gate insulating film having a thickness of about 1000Å. As shown in Figs. 2A and 2B, a normal I-V curve is obtained when the polysilicon thin film transistor is operated for the first time. However, for the second and operations thereafter, the I-V curve shifts progressively and rarely overlaps. Since the I-V operating curve of a conventional polysilicon thin film transistor is highly non-repetitive, reliability of a conventional polysilicon thin film transistor device is usually poor.

SUMMARY OF INVENTION

[0010] Accordingly, one object of the present invention is to provide a polysilicon thin film transistor having an improved reliability of operation and performance.

[0011] A second object of this invention is to provide a polysilicon thin film transistor capable of tracing out an overlap-

ping current/voltage (I-V) curve during repeated operation.

[0012] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a polysilicon thin film transistor over a substrate. The polysilicon thin film transistor includes a poly-island layer having a channel region and a doped source/drain region on each side of the channel region, a gate, a gate insulating film comprising an oxide layer and a nitride layer and an inter-layer dielectric (ILD). The gate is positioned over the poly-island layer. The oxide layer is formed between the gate and the poly-island layer and the nitride layer is formed between the gate and the oxide layer. The inter-layer dielectric includes a first inter-layer dielectric and a second inter-layer dielectric. The first inter-layer dielectric covers the gate and the nitride layer while the second inter-layer dielectric covers the first inter-layer dielectric. A source/drain contact is embedded between the first inter-layer dielectric and the gate insulating film on each side of the gate. The source/drain contact is electrically connected to the doped source/drain region of the poly-island layer.

[0013] The polysilicon thin film transistor according to this in-

vention employs a gate insulating film that includes an oxide layer and a nitride layer. The composite gate insulating film reinforces the repeatability of electrical characteristics in repeated operations and hence improves transistor reliability.

[0014] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

Brief Description of Drawings

[0015] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0016] Fig. 1 is a schematic cross-sectional view of a conventional polysilicon thin film transistor.

[0017] Figs. 2A and 2B are graphs showing the relationship between drain current (I_D) and gate voltage (V_G) of two conventional polysilicon thin film transistors each having a different poly-island aspect ratio obtained after repeated operations.

[0018] Fig. 3 is a schematic cross-sectional view of a polysilicon thin film transistor according to one preferred embodiment of this invention.

[0019] Figs. 4A and 4B are graphs showing the relationship between drain current (I_D) and gate voltage (V_G) of two polysilicon thin film transistors each having a different poly-island aspect ratio obtained after repeated operations, wherein the polysilicon thin film transistors are fabricated according to this invention with the gate insulating film comprising a nitride layer having a thickness of about 200Å and an oxide layer having a thickness of about 1000Å.

[0020] Figs. 5A and 5B are graphs showing the relationship between drain current (I_D) and gate voltage (V_G) of two polysilicon thin film transistors each having a different poly-island aspect ratio obtained after repeated operations, wherein the polysilicon thin film transistors are fabricated according to this invention with the gate insulating film comprising a nitride layer having a thickness of about 400Å and an oxide layer having a thickness of about 1000Å.

DETAILED DESCRIPTION

[0021] Reference will now be made in detail to the present pre-

ferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0022] Fig. 3 is a schematic cross-sectional view of a polysilicon thin film transistor according to one preferred embodiment of this invention. The polysilicon thin film transistor (TFT) 30 includes a poly-island layer 302, a composite gate insulating film 305 comprising of a silicon oxide layer 303 and a silicon nitride layer 304, a gate 306 and a first and second inter-layer dielectric 308, 309 over a substrate 300. The poly-island layer 302 includes a channel region 302a under the gate 306 and a doped source/drain region 302b such as a P-doped region or an N-doped region on each side of the channel region 302a. A lightly doped drain (LDD) 302c may also be formed between the channel region 302a and the doped source/drain region 302b. In addition, the nitride layer 304 in the gate insulating film 305 has a thickness between about 50Å to 400Å and the oxide layer 303 has a thickness between 100Å to 1400Å.

[0023] As shown in Fig. 3, the gate 306 is formed over the chan-

nel region 302a. The oxide layer 303 of the gate insulating film 305 is formed between the gate 306 and the poly-island layer 302. The oxide layer 303 preferably has a thickness smaller than 1400Å. The nitride layer 304 of the gate insulating film 305 is formed between the gate 306 and the oxide layer 303. The nitride layer 304 preferably has a thickness smaller than 400Å. The first inter-layer dielectric 308 covers the gate 306 and the gate insulating film 305. A source/drain contact metal 310 is also embedded between the first inter-layer dielectric 308 and the gate insulating film 305 on each side of the gate 306. The source/drain contact metal 310 is electrically connected to the doped source/drain region 302b. The second inter-layer dielectric 309 is formed over the transistor. Furthermore, to prevent the diffusion of impurities from the glass substrate 300 of a thin film transistor liquid crystal display, a buffer layer 301 is often formed directly over the substrate 300.

[0024] To indicate the improvement in reliability of the polysilicon thin film transistor of this invention relative to a conventional design, refer to Figs. 4A and 4B. Figs. 4A and 4B are graphs showing the relationship between drain current (I_D) and gate voltage (V_G) of two polysilicon thin film tran-

sistors each having a different poly-island aspect ratio obtained after repeated operations. The polysilicon thin film transistors are fabricated according to this invention with the gate insulating film comprising a nitride layer having a thickness of about 200Å and an oxide layer having a thickness of about 1000Å. During operation, a voltage of about 10V is applied to the drain terminal (V_D). As shown in Figs. 4A and 4B, the I-V curve is able to maintain at a fixed position for a poly-island layer at a width/length ratio of 30/6 or 60/6 under repeated operations. Thus, compared with the I-V curve in Figs. 2A and 2B with large shifting after repeated operations, reliability of the polysilicon thin film transistor fabricated according to this invention is improved considerably.

[0025] When the nitride layer in the polysilicon thin film transistor fabricated according to this invention is increased to 400Å, the I-V curve after repeated operation of the transistor is shown in Figs. 5A and 5B. As shown in Figs. 5A and 5B, the I-V curve is more stable as the nitride layer is increased from 200Å (in Figs. 4A and 4B) to 400Å. With a thicker nitride layer, the capacity of the polysilicon thin film transistor to withstand stress is increased and hence overall reliability of the transistor is further improved.

Since the I-V curve of the polysilicon thin film simply overlaps on repeated operations as thickness of the nitride layer is increased to 400Å and increasing the thickness of the nitride layer has minor effect on device miniaturization, the nitride layer is preferably set to around 400Å.

[0026] In conclusion, one major aspect of the polysilicon thin film transistor according to this invention is that a composite gate insulating film comprising of an oxide layer and a nitride layer is deployed. The composite gate insulating film reinforces the repeatability of electrical characteristics in repeated operations so that performance and reliability of the transistor is improved.

[0027] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.